Optimization of Front-End Design in Imaging and Spectrometry Applications With Room Temperature Semiconductor Detectors

Lorenzo Fabris and PierFrancesco Manfredi

***Abstract*—This paper addresses the optimization of front-end design in position sensing, imaging. and high-resolution energy dispersive analysis with room temperature semiconductor detectors. The focus is on monolithic solutions able to meet the requirements of high functional densities set by multielectrode, finely segmented detectors. Front-end architectures featuring additional functions besides charge measurements, as demanded by the need of acquiring and processing multiparametric information associated with the detector signals will be discussed. Noise will be an issue of dominant importance in all the following analysis. The advent of CMOS processes featuring submicron gate length and gate oxide thicknesses in the few nanometers region is overturning some of the classical criteria in the choice of the front-end device. The achievement of the limits in resolution requires a strict control of the noise contribution from the current amplifier which ordinarily follows the front-end element in the charge-sensitive loop. This aspect becomes more crucial in designing front-end systems with submicron processes.**

***Index Terms*—Capacitive matching, monolithic processes, noise optimization.**

I. Introduction

THERE are at least four reasons to suggest that the criteria underlying the front-end design should be reconsidered.

The first reason is related to the growing number of imaging applications, requiring a high spatial resolution at high rates of events. This reflects into the demand for more finely segmented pixel and strip detectors, readout by low noise, high-density front-end systems, that in some cases may also be required to be radiation hard [1]–[8]. The second reason is that several applications are based upon a time-correlated image buildup so the front-end system may be requested to provide accurate timing features along with a high-resolution spatial definition [9], [10].

The third reason is connected with front-end systems intended for spectrometry applications. The fourth one is the need of assessing the benefits brought about to the front-end design by the advancement in the monolithic technologies, especially in the MOSFET area [11]–[15]. The most advanced MOSFET processes feature a gate length of a fraction of a micron and a thickness of the gate oxide in the few nanometers region. The resulting benefits in analog applications are related to the achievement of better transconductance-to-standing-current ratios and to a reduced low-frequency noise in the channel current [16]–[19].

The progress in the MOSFET processes is modifying the criteria that govern the choice of the front-end element and changing the regions of detector capacitances and peaking time values where the MOSFET outperforms or under performs the silicon junction field-effect transistor (JFET) in low-noise applications.

When the main goal is the achievement of the limits in the noise behavior of a front-end system based on either type of component, a thorough control of all the additional noise contributions becomes of paramount importance. Some of these contributions will be discussed in this paper. For instance, the minimization of the contribution added by the current preamplifier which follows the front-end device in a charge-sensitive loop becomes an important issue. It might be argued that such a contribution is a second order effect. If this may be true, it is certainly true, however, that the second-order effects may be the real limitation to the achievement of the target noise performances. It should be pointed out that these additional noise contributions become more important in a preamplifier using a submicron input device. It will be shown how these considerations affect the design of the input device itself.

II. Basic Architectures of the Front-End System

A front-end system intended to acquire and process signals from a multielectrode detector has an input analog section which consists of as many channels as the incoming signals. Basic components of each channel are the front-end amplifier, in most cases a charge-sensitive loop and the shaper. The further processing of the shaped signal depends on the particular function the system must implement. Some examples are given in Fig. 1.

In the simplest case the shaper is followed by a threshold comparator, which detects the presence of a signal carrying a charge above a preset value, case a) in Fig. 1. Several imaging systems employing pixel or strip detectors are based on this simple function [20]–[23]. In other applications the charge information must be retained. This is the case, for instance, when a space resolution beyond the intrinsic geometric limits of the segmentation must be obtained by a centroid evaluating algorithm. The charge can be stored in an analog memory, like in case c) of

Manuscript received November 24, 2001; revised May 16, 2002. This work was supported by the Director, Office of Science, Office of Basic Energy Sciences, of the U.S. Department of Energy under Contract DE-AC03-76SF00098.

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Digital Object Identifier 10.1109/TNS.2002.801703

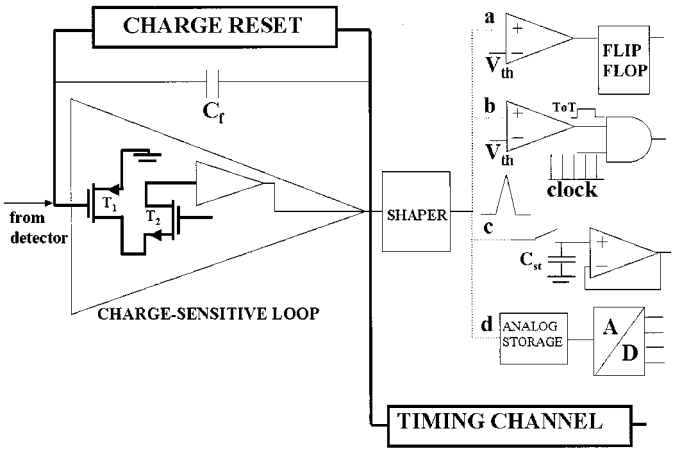

Fig. 1. Basic architectures of the analog section in a front-end system.

Fig. 1. This solution is pursued, for instance, when the centroid algorithm is realized by analog methods.

Alternatively, the stored value of the charge can be converted into a number and the centroid calculated on the basis of the numerical values, case d) in Fig. 1.

A simple way of arriving at a digital evaluation of the input charge is based on the principle of time-over-threshold (ToT) [24], [25], shown as case b) in Fig. 1. This is a compression-type, nonlinear transformation of the amplitude at the shaper output into a time variable, represented by the duration of the signal at the comparator output. Such duration is converted into a number by classical techniques of time-to-digital conversion.

As shown in Fig. 1, a timing channel can be derived from the preamplifier output. This feature is becoming more and more important with the growing request of time-correlated imaging in some chemistry and biology studies. Besides, three-dimensional imagers based on time-domain reflectometry have been obtained from two-dimensional imaging systems by associating an accurate timing channel with each pixel.

The elements highlighted by thicker lines in Fig. 1 constitute the crucial aspects in the front-end design. The first one is the input circuit in the charge-sensitive preamplifier, which determines to a large extent the noise behavior of the channel. This sets the most important limit to the accuracy in both charge measurement and time definition. Focus on this aspect will be in Section III. The second one is the reset circuit in the charge-sensitive loop. An excellent analysis of the solutions realizable in CMOS technology is provided in [26]. The third one is the timing channel. Description of an accurate timing circuit can be found in [27].

III. Noise Optimization in Monolithic Design

A. Choice of the Type of Front-End Device

As pointed out in Section I, the evolution in CMOS technologies associated with the device scaling is, if not overturning, certainly modifying the choice criteria of the front-end element in the charge-sensitive loop. In a nutshell, a top quality P-channel MOSFET may invade a good portion of the region of applications which was conventionally covered by the JFET.

To discuss these aspects in more detail, three monolithic technologies are considered in this section. One is a CMOS process featuring 0.25-μm minimum gate length $L_{\min}$ and an oxide thickness of 5 nm [16], [17]. The other two technologies offer a JFET as a front-end element. Of these two technologies, one, DMILL, is a BiCMOS-JFET process whose JFET is P-channel. [28]–[30].

The second is entirely based on top quality, spectrometry grade N-channel JFETs. [31], [32]. The technologies featuring complementary MOSFETs are more flexible and therefore more suited for a design requiring a variety of analog and digital functions.

The noise behavior dictates the choice of the front-end device, either an N or P-channel MOSFET in a CMOS process, N or P-channel MOSFET or a P-JFET in a DMILL-based design. The further possibility in the DMILL case, the bipolar transistor is neglected here, as its use is restricted to very specific, though important applications. In some circumstances the noise may even drive the choice of the technology, for instance directing the preference to the process featuring the NJFET as a sole active element. In this case the front-end chip will be restricted to the preamplification function, all other processing being transferred to a separate CMOS chip.

In charge measurements, the noise characteristics of the front-end systems are currently expressed by the equivalent noise charge (ENC). The dominant contribution to ENC usually comes from the so-called series or voltage noise, which is mostly due to the noise associated with the drain current in the input device. In the following analysis, this will be considered ideally to be the only source of noise in the front end. For the sake of reference, it is assumed that the cascade connection of preamplifier and shaper responds to a delta-impulse injected at the preamplifier input with a symmetric piecewise parabolic weighting function of peaking time t_p. The noise coefficients of such a weighting function are: $A_1 = 1.33$ for the series noise component with frequency dependence f^0, $A_2 = 0.57$ for the series noise component with frequency dependence f^{-1} and $A_3 = 0.39$ for the series noise component with frequency dependence f^{-2}. The ENC is evaluated from the gate referred spectral power densities of the channel current noise given by (1) for a MOSFET and by (2) for a JFET [41]

$$S_M(f) = S_{0,M} + \frac{K_f}{f^\alpha} \quad (\alpha = 1) \tag{1}$$

$$S_J(f) = S_{0,J} + \frac{K_L}{f^2}. \tag{2}$$

In (1) and (2) $S_{0,M}$ and $S_{0,J}$ are the power densities of the series noise with frequency dependence f^0 in a MOSFET and in a JFET. K_f is the coefficient of $1/f$ noise in the MOSFET and K_L is the low-frequency noise parameter in the JFET.

In a low noise JFET $S_{0,J}$ can be considered as entirely determined by the channel thermal noise and expressed as $(8/3)kT/g_m$, where g_m is the transconductance of the device, k is Boltzmann's constant and T the absolute temperature. $S_{0,M}$ in MOSFETs contains additional terms besides the channel thermal noise and so does $S_{0,J}$ in some JFETs belonging to

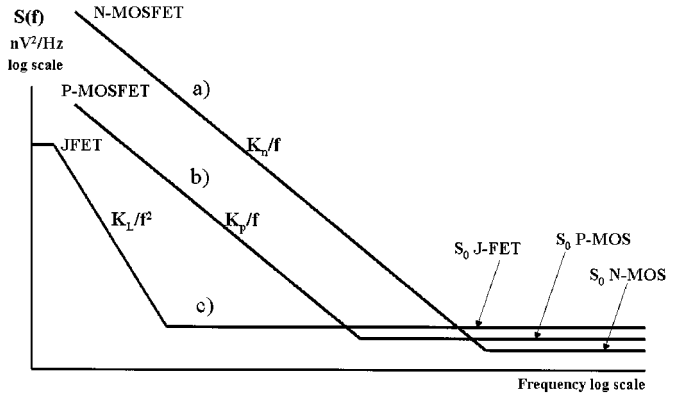

Fig. 2. Conceptual behavior of the $S(f)$ power density as a function of frequency. a) N-channel MOSFET belonging to a submicron CMOS monolithic process. b) P-channel MOSFET belonging to a submicron CMOS monolithic process. c) N-channel JFET belonging to a classical JFET monolithic process.

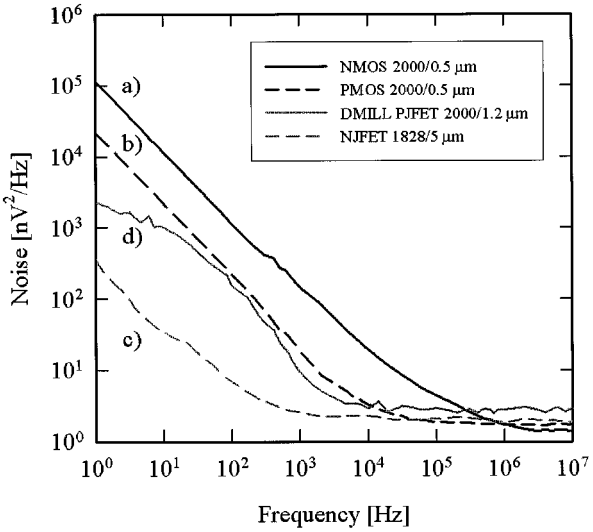

Fig. 3. Frequency dependence of the $S_M(f)$, $S_J(f)$ spectral power densities for devices belonging to different monolithic processes. a) N-channel MOSFET belonging to a CMOS process featuring $L_{\min} = 0.25\ \mu$m, $t_{ox} = 5$ nm, actual gate length $L = 0.5\ \mu$m, drain current $I_D = 0.5$ mA, input capacitance $C_i = 6$ pF. b) P-channel MOSFET belonging to the same CMOS process as above, actual gate length $L = 0.5\ \mu$m, drain current $I_D = 0.5$ mA, input capacitance $C_i = 6$ pF. c) N-channel JFET belonging to an all N-JFET monolithic process, actual gate length $L = 5\ \mu$m, input capacitance $C_i = 10$ pF, drain current $I_D = 5$ mA. d) P-channel JFET belonging to DMILL BiCMOS JFET process, actual gate length $L = 1\ \mu$m, input capacitance $C_i = 9$ pF, drain current $I_D = 1$ mA.

JFET-CMOS processes like, for instance DMILL. However, for the purpose of the following analysis, an adequate approximation is the one which represents $S_{0,M}$ as $4kT\Gamma(1/g_m)$, where Γ is a coefficient ordinarily of the order of unity, which, however, may become consistently larger than 1 in short channel MOSFETs operating in strong inversion.

Equations (1) and (2) also highlight the difference in the low-frequency noise mechanism of the two types of device. In MOSFETs the low-frequency region of the noise spectrum is governed by $1/f$ noise [33]. The term which appears in (2) to describe the low-frequency noise in a JFET is approximated as the tail of a Lorentzian distribution. Such an approximation is valid for low noise JFETs in most of practical applications and fails only in devices exposed to a substantial dose of radiation.

A conceptual comparison of the relative merits of N and P-channel MOSFETS belonging to the same process and an N-channel JFET, all assumed to be of identical C_i values, is provided by the model plots of Fig. 2. The MOSFETs behavior is typical of a submicron process with gate oxide thickness in the 5-nm region. The JFET behaves as a device belonging to a classical low-noise monolithic process with a few micron gate length.

The plots aim at pointing out that, of the three considered devices, the N-channel MOSFET has the smallest high-frequency noise, while usually the JFET has the best behavior in the low-frequency region. However, as compared to MOSFETS of the previous generations, the new MOSFET processes feature a considerable improvement in their $1/f$ noise governed low-frequency behavior. To understand the reasons for this, it should be remembered that the coefficient K_f of $1/f$ noise in a MOSFET can be expressed as

$$K_f = \frac{K_a}{(C_i \cdot C_{\text{ox}})} \tag{3}$$

where K_a depends on the quality of the gate oxide and on the height of the barrier at the junction Si/SiO_2 and C_{ox} is the gate-to-channel capacitance per unit area.

The reduction in the gate oxide thickness and a likely improvement in the oxide quality have resulted in a substantially lower $1/f$ noise in the most advanced MOSFET processes. Still, the P-channel features less $1/f$ noise than the N-channel MOSFET, as pointed out in Fig. 2. The ratio $K_{f,N}/K_{f,P}$ depends on the process and can vary from a minimum of a few units to a maximum of about 30.

The expressions of ENC^2 are given by (1) for the MOSFET and by (2) for a JFET [41]

$$\text{ENC}_M^2 = (C_D^* + C_i)^2 \cdot \left[\frac{A_1 S_{0,M}}{t_p} + 2\pi K_f A_2\right] \tag{4}$$

$$\text{ENC}_J^2 = (C_D^* + C_i)^2 \cdot \left[\frac{A_1 S_{0,J}}{t_p} + K_L A_3 t_p\right]. \tag{5}$$

In the previous equations, C_D^* is the sum of all open-loop capacitances shunting the preamplifier input, including the detector capacitance C_D, the feedback capacitance C_f in the charge-sensitive loop and strays. C_i is the input capacitance of the front-end device.

The actual power densities of the series noise relevant to four devices, all of gate width W in the 2000-μm region are plotted as functions of frequency in Fig. 3. The devices are: an N-channel and a P-channel MOSFET belonging to the same CMOS process, featuring a minimum gate length $L_{\min} = 0.25\ \mu$m and a gate oxide thickness $t_{\text{ox}} = 5.5$ nm, an N-channel JFET part of a monolithic low-noise JFET technology and the P-channel JFET belonging to the DMILL process. The frequency spectra of Fig. 3 were made at equal ratios between

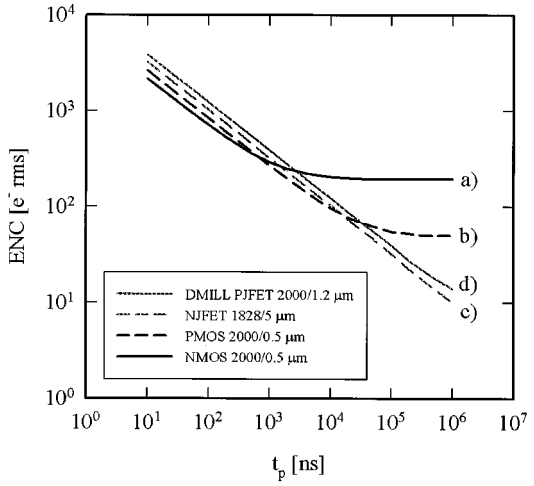

Fig. 4. ENC versus t_p plots for the four devices of Fig. 3. a) ENC_M versus t_p dependence for the N-MOS. b) ENC_M versus t_p dependence for the P-MOS. c) ENC_J versus t_p dependence for the N-JFET and d) ENC_J versus t_p dependence for the DMILL P-JFET.

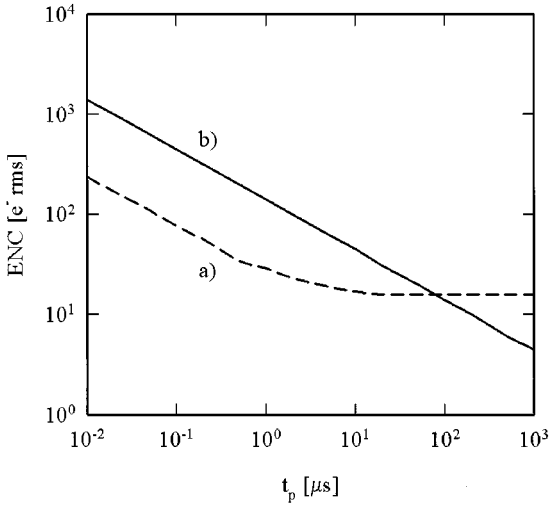

Fig. 5. ENC as a function of the peaking time t_p. a) P-MOS, $C_i = 110$ fF, detector capacitance $C_D^* = 330$ fF. b) N-JFET, $C_i = 1$ pF, detector capacitance $C_D^* = 3.3$ pF.

drain current I_D and gate length L [16], [17], [26], [28]. The reason for this assumption can be explained as follows.

Supposing the devices described by a square-law dependence of their drain current on the gate-to-source voltage, their transconductance, which determines the channel thermal noise is proportional to $(I_D/L)^{1/2}$. Therefore, the assumption of constant I_D/L serves the purpose of pointing out that a reduction in channel length allows a proportional decrease in drain current to achieve the same transconductance.

The relevant ENC versus t_p plots, evaluated under the assumption that each of the four devices is employed as the front-end element of a charge-sensitive loop with a 1-pF feedback capacitance C_f, associated with a 20-pF detector are given in Fig. 4. These values tend to represent the case of a strip detector with long strips in an application where the preamplifier is required to have a short-rise time. It may alternatively represent the case of a spectrometry application with a planar detector of active area in the cm^2 region. The curves of Fig. 4 were obtained by introducing the values of the noise parameters determined on the basis of Fig. 3 into (1) and (2).

The following important conclusions can be drawn from Fig. 4. At short peaking times, t_p below about 100 ns the N-MOS is to be preferred. As t_p approaches the 1-μs region the P-MOS outperforms all the other devices. This is probably the most striking consequence of the improvement in the CMOS area, in the sense that the P-MOS tends to invade the area which used to be restricted to the JFET. The JFETs, by virtue of their superior behavior in the low-frequency region, are still unsurpassed at peaking times in the 10-μs domain.

At these peaking time values the gate leakage current in a JFET does not yet constitute a serious limitation, therefore, spectrometry measurements where the counting rate aspect can be compromised in favor of the highest possible energy resolution will continue to be based on the JFET. Of the two JFETs considered in Figs. 3 and 4 the N-cannel device has better performances than the DMILL P-channel JFET throughout the explored interval of t_p values. However, also the DMILL P-JFET outperforms the MOSFETs at very long peaking times. As Fig. 4 points out, there is a crossover point at a critical value t_p^* in the ENC versus t_p curves relevant to the N and P-channel MOSFETs. Considering an N and P-channel MOSFET of equal input capacitance operating at the same current in the same inversion region, t_p^* is given by

$$t_p^* = A_1 \cdot \frac{S_{0,MP} - S_{0,MN}}{2\pi A_2 \left(K_{f,N} - K_{f,P}\right)}. \tag{6}$$

It is interesting to show the noise limits achievable now in applications with detectors of small capacitance. The situations considered here refer to two real detector-front-end combinations, one relevant to a pixel case, the second one to a silicon detector with short strips, 3 cm in length. The matching condition employed in both cases is $C_i = C_D^*/3$, which provides the minimum ENC under the constraint of fixed drain current. In the pixel case, Fig. 5(a), $C_D^* = 330$ fF and the detector is supposed to be associated with a P-MOS front-end element, featuring $W = 100\ \mu$m, $L = 0.35\ \mu$m, $C_i = 110$ fF.

Plot b) in the same figure shows the noise limits presently achievable with a preamplifier using a small input JFET ($C_i =$ 1 pF) based on the same process as the N-channel device in Fig. 3. The detector capacitance in the case of the short strips is $C_D^* = 3.3$ pF.

The noise description based upon the spectral power density such as that of Fig. 3, if useful in characterizing the noise features of a particular device is of little use in evaluating the ENC when a device belonging to a given process is scaled up or down in W to match the actual detector capacitance. For this purpose it is better to provide the frequency dependence of the products

$$C_i S_M(f) = C_i S_{0,M}(f) + \frac{C_i K_f}{f} \tag{7}$$

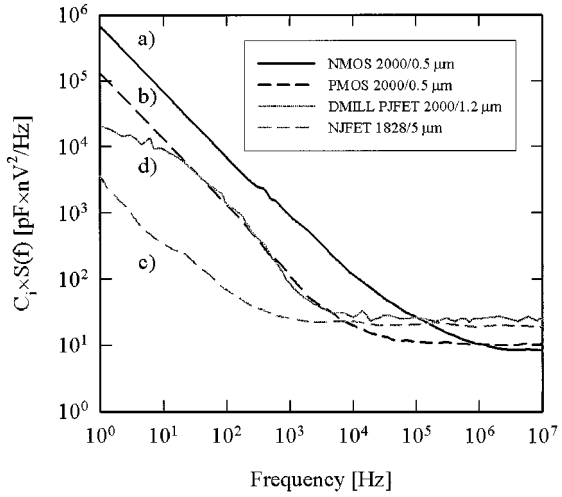

Fig. 6. Frequency dependence of the $C_iS_M(f)$ and $C_iS_J(f)$ products for the four devices considered in Fig. 3. a) Frequency dependence of $C_iS_M(f)$ for the N-MOS. b) Frequency dependence of $C_iS_M(f)$ for the P-MOS. c) Frequency dependence of $C_iS_J(f)$ for the N-JFET. d) Frequency dependence of $C_iS_J(f)$ for the DMILL P-JFET.

for the MOSFET and

$$C_iS_J(f) = C_iS_{0,J}(f) + \frac{C_iK_L}{f^2} \tag{8}$$

for the JFET.

The parameters K_f, K_L describing the $1/f$ noise in a MOSFET and the $1/f^2$ noise in a JFET are inversely proportional to C_i. This means that in devices belonging to the same process, featuring the same gate length L, the gate-referred $1/f$ and $1/f^2$ densities reduce as the gate width W is increased. It is useful, therefore, to introduce $H_f = C_iK_f$ and $H_L = C_iK_L$ as characteristic, W-independent parameter of $1/f$ noise in a MOSFET and $1/f^2$ noise in a JFET. The products $C_iS_{0,M}(f)$ and $C_iS_{0,J}(f)$ are W-independent if two conditions are met as follows:

a) S_0 is mostly governed by the channel thermal noise;

b) scaling in W is done at constant current density.

The previous condition a) is more likely to be met in JFETs than in MOSFETs. When they are satisfied, $C_iS_{0,M}(f)$ and $C_iS_{0,J}(f)$ are W-independent and the noise behavior of all the devices belonging to the same process is known from a noise spectral measurement done on a single device of known capacitance. The $C_iS_M(f)$ and $C_iS_J(f)$ products for the four devices considered in Fig. 3 are plotted in Fig. 6.

Compared to the plots of Fig. 3, those in Fig. 6 provide a normalized description of the noise behavior of an active device that is C_i-independent and, as such, they are more adequate to describe the noise behavior of an active device in detector applications than the plots of Fig. 3. For instance, from Fig. 3 it is difficult to infer why the N-JFET has considerably worse ENC than the P-MOS at short peaking times, as apparent in Fig. 4. According to Fig. 3, indeed, the difference in their high-frequency power densities is small. The true reason for the different ENC behavior at short t_p values is that, although the two devices have high-frequency noise power densities close in value, the N-JFET has a consistently larger C_i. This aspect is clearly pointed out by the curves of Fig. 6.

Besides, the knowledge of $C_iS_M(f)$ and $C_iS_J(f)$ allows a straightforward determination of the normalized ENC values from

$$\frac{\mathrm{ENC}_M}{\left[(C_D^*)^{1/2}\cdot\left(m+\frac{1}{m}\right)\right]} = 6.25\left[\frac{A_1C_iS_{0,M}}{t_p} + 2\pi H_fA_2\right]^{1/2} \text{electrons}/(\text{pF})^{1/2} \tag{9}$$

$$\frac{\mathrm{ENC}_J}{\left[(C_D^*)^{1/2}\cdot\left(m+\frac{1}{m}\right)\right]} = 6.25\left[\frac{A_1C_iS_{0,J}}{t_p} + 2\pi H_LA_3t_p\right]^{1/2} \text{electrons}/(\text{pF})^{1/2}. \tag{10}$$

In the previous equations $m = (C_D^*/C_{i,a})^{1/2}$ is the mismatch factor in the actual case, that is, as determined by a device with an input capacitance $C_{i,a}$ generally different from C_i, the input capacitance of the sample device on which the power spectral density is measured. In (9) and (10), the capacitances are expressed in pF, $C_iS_{0,M}$ and $C_iS_{0,J}$ in pF $\times$ (nV^2/Hz) and t_p in μs.

B. Choice of the Optimum Size of the Front-End Device

The considerations about the optimum size of the front-end device, as they are available in the literature, are usually done under the hypothesis that the noise is determined by the sole input device. It will be shown in the following that the noise in the current amplifier which follows the front-end element in the charge-sensitive loop affects the optimization process of the input device itself. Therefore, the optimization process should involve the entire input circuit in the charge-sensitive loop, which in its simplest version is a cascode. However, as a first step it is useful to review the classical optimization procedure, which is named, though improperly, "capacitive matching." In a preamplifier, where the only noise sources are those associated with the main current in the input active device, the optimum size condition depends on the constraints under which the scaling of the device is done [34]–[36].

1) The Scaling is Done Keeping the Linear Current Density I_D/W Constant: The I_D/W ratio determines to a large extent the inversion condition in a MOSFET. Therefore, if the current in the device is scaled with W so that the current density remains constant, the inversion condition in a MOSFET should remain the same.

In this case, it can be reasonably assumed that $C_iS_M(f)$ and $C_iS_J(f)$ as given by (7) and (8) are independent of W. This may be not strictly true in MOSFET circuits, but the resulting inaccuracy is tolerable in most cases. As a consequence of this hypothesis, the transition frequency $\omega_T = g_m/C_i$ is a constant. The square brackets at the second member of (9) and (10)

are, accordingly, independent of C_i and the condition of minimum ENC occurs when $C_i = C_D^*$, which is the true capacitive matching condition.

2) The Scaling is Done Keeping the Drain Current I_D Constant: This is the situation where the value of the drain current is constrained and must be kept fixed as W and C_i along with it are scaled. By rewriting (1) and (2) in the following way:

$$\mathrm{ENC}_M^2 = \left[\frac{(C_D^* + C_i)^2}{C_i}\right] \cdot \left[\frac{4kT \cdot \left(\frac{C_i}{g_m}\right) A_1}{t_p} + 2\pi H_f A_2\right] \tag{11}$$

$$\mathrm{ENC}_J^2 = \left[\frac{(C_D^* + C_i)^2}{C_i}\right] \cdot \left[\frac{4kT \cdot \left(\frac{C_i}{g_m}\right) A_1}{t_p} + H_L A_3 t_p\right] \tag{12}$$

and remembering that the terms $2\pi H_f A_2$ and $H_L A_3 t_p$, are independent of C_i, their contributions to ENC attain a minimum at the C_i value which minimizes the first square bracket in (11) and (12), that is, $C_i = C_D^*$. The minimization of the contribution due to the channel thermal noise requires that the relationship between g_m and C_i be made explicit. In the case of a MOSFET operating in strong inversion g_m is proportional to $C_i^{1/2}$ and this results in the condition of minimum ENC contribution due to channel thermal noise at $C_i = C_D^*/3$. Therefore, in a MOSFET operating under the constraint of fixed current, the value of C_i, which minimizes ENC_M^2 lies in the interval

$$\frac{C_D^*}{3} < C_i < C_D^*. \tag{13}$$

Its exact value depends on the relative weight of thermal and $1/f$ noise in determining ENC_M^2.

The same condition of minimum channel thermal noise contribution to ENC: $C_i = C_D^*/3$ is obtained in the case of a JFET operating at a current lower that its I_{DSS}, being I_{DSS} the drain current at zero gate-to-source voltage.

In a MOSFET operating in moderate inversion the lower limit of inequality (13) is smaller than $C_D^*/3$ [37].

In a MOSFET operating in weak inversion g_m depends exclusively on I_D and is independent of W and L. Therefore, the constraint set on I_D fixes the value of g_m. It is therefore advisable to employ the smallest W which retains the adopted inversion condition at the preset current [26].

3) Further Considerations on the Optimum Size of the Input Device: As a comment to the capacitive matching condition, $C_i = C_D^*$ it is worth pointing out that the condition of device scaling at constant current density is not essential. In order that $C_i = C_D^*$ be the condition which minimizes the channel thermal noise it is required that g_m be proportional to C_i. A typical situation of this type is that of a MOSFET operating in condition of velocity saturation, where $g_m = C_{\mathrm{ox}} W L v_{\mathrm{sat}}/L$, v_{sat} being the saturation velocity.

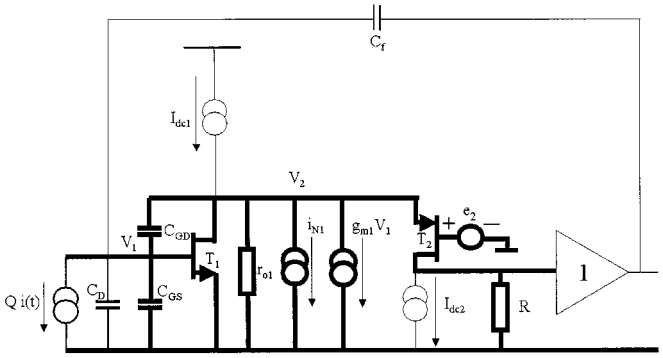

Fig. 7. Model of charge-sensitive loop.

C. Effect of the Noise in the Current Amplifier Which Follows the Input Device

As anticipated, the noise associated with the current amplifier that follows the input device affects the design of the front-end device itself. To discuss this point, the charge-sensitive loop shown in Fig. 7 will be considered.

The circuit in Fig. 7 is an oversimplified schematic which puts into evidence the input cascode, made of transistors T_1 and T_2, followed by an ideal buffer. The thicker lines highlight the circuit elements that intervene in signal and noise analysis. The dc current sources I_{dc1} and I_{dc2} have been shown for the sake of completeness, although they are inessential in this analysis. The active behavior of T_1 is described by the voltage-controlled current source $g_{m1}V_1$, where g_{m1} is the transconductance of T_1. The model of T_1 is completed by its gate-to-source and gate-to-drain capacitances C_{GS} and C_{GD} and by its drain-to-source dynamic resistance r_{o1}. The current source i_{N1} represents the noise associated with the drain current in T_1 and the noise of T_2 is described by the voltage source e_2. The detector is represented by the current source $Q \times i(t)$ in parallel to the capacitance C_D. An extremely large open-loop gain will be assumed in the charge-sensitive loop.

The dominant terms in the spectral power density $d\langle V_{0,N}^2\rangle/df$ of the noise at output of the charge sensitive loop are described by

$$\frac{d\langle V_{0,N}^2\rangle}{df} = \left[\frac{(C_D^* + C_i)^2}{g_{m1}^2 \cdot C_f^2}\right] \cdot \left[\frac{d\langle i_{N,1}^2\rangle}{df} + \left(\frac{1}{r_{o1}} + \frac{g_{m1} \cdot C_{\mathrm{GD}}}{(C_D^* + C_i)}\right)^2 \cdot \frac{d\langle e_2^2\rangle}{df}\right] \tag{14}$$

where $C_D^* = C_D + C_f$ and $C_i = C_{\mathrm{GS}} + C_{\mathrm{GD}}$.

The term $G = (1/r_{01}) + g_{m1}C_{\mathrm{GD}}/(C_D^* + C_i)$ whose square multiplies the gate referred spectral density $d\langle e_2^2\rangle/df$ of T_2 is the dynamic conductance appearing on the drain of T_1. G determines the impact of the noise of T_2 on the total noise at the preamplifier output. A first consideration that can be made on the basis of (14) is that a reduction in the gate length L of T_1, causes a decrease in r_{o1}, and a related increase in G. This is one more reason why deep submicron MOSFETS, that is, devices with L below approximately 0.3 μm are not advisable as front-end elements in charge-sensitive loops.

Numerical evaluations show, however, that unless extremely small values of L are used, the dominant term in G is $g_{m1}C_{\rm GD}/(C_D^* + C_i)$, which is due to the capacitive feedback around T_1. To give a numerical example, a PMOS with $W = 2000$ μm and $L = 0.35$ μm would feature at a 300 μA drain current $g_m = 6$ mS, $C_i = 4$ pF and $C_{\rm GD} = 1.35$ pF. Employed as the front-end device in a charge-sensitive preamplifier coupled to a detector of 4 pF, that is the condition of capacitive matching, the value of the term $g_{m1}C_{\rm GD}/(C_D^* + C_i)$ would be 1.01 mS. The corresponding resistance, 990 Ω appears in parallel to r_{o1}, whose value in this case is 1.6×10^4 Ω. This example confirms the previous statement that the dominant component of G is the one determined by the capacitive feedback around T_1. Such a large value of G makes the contribution of T_2 to the total ENC nonnegligible, as shown by (15), which refers to the case where T_1 and T_2 are MOSFETs

$$\mathrm{ENC}_M^2 = \left[4kT\Gamma\left(\frac{1}{g_{m1}}\right)\cdot\frac{A_1}{t_p} + 2\pi K_f A_2\right]\cdot(C_D^* + C_i)^2 + \eta^2 C_i^2\left[4kT\Gamma\left(\frac{1}{g_{m2}}\right)\cdot\frac{A_1}{t_p} + 2\pi K_f A_2\right]. \quad (15)$$

In (15), $C_{\rm GD}$ has been represented as ηC_i. The presence of the $\eta^2 C_i^2$, besides defining the contribution brought about by the noise in T_2 to the total ENC has the effect of modifying the choice of the optimum size for T_1. As an example, the case will be considered where the noise in T_1 and T_2 is restricted to the channel thermal noise for which (15) simplifies into

$$\mathrm{ENC}_M^2 = 4kT\Gamma\frac{A_1}{t_p}\left[\frac{(C_D^* + C_i)^2}{\omega_T C_i} + \eta^2 C_i^2\left(\frac{1}{g_{m2}}\right)\right] \quad (16)$$

where $\omega_T = g_{m1}/C_i$ is the transition angular frequency of T_1. For T_1 the following values of ω_T and η^2 are assumed: $\omega_T = 1.5$ Grad/s, $\eta^2 = 0.14$ and g_{m2} made equal to 1 mS. The same value $C_D^* = 21$ pF employed in the ENC evaluations of Fig. 4 will be utilized here and t_p assumed to be 100 ns. The dependence of ENC_M^2 on the ratio C_i/C_D^* is plotted in Fig. 8 in both cases of 1) absence and 2) presence of noise in T_2.

In absence of noise due to T_2, ENC_M^2 attains its minimum at $C_i/C_D^* = 1$, as expected in the actual situation of C_i scaling at constant current density. In presence of the noise due to T_2, the minimum in ENC_M^2 occurs at a consistently smaller value in C_i/C_D^*. Besides, owing to the $\eta^2 C_i^2$ term, ENC_M^2 rises more sharply as C_i/C_D^* increases beyond the optimum value. Therefore, if T_1 is designed to meet the matching condition C_i/C_D^*, the presence of T_2 noise would degrade ENC_M^2 to a nonnegligible extent. If the $1/f$ noise in T_1 and T_2 is considered, a common practice, which consists in choosing a P-channel device for T_1 and an N-channel device for T_2 has the disadvantage of a sizeable increase in the term due to $1/f$ noise, whose constant K_a is larger in an N-MOS than in a P-MOS. To circumvent this problem, either the complementary cascode is avoided and replaced by a cascode made of two transistors of the same type or the active cascode solution of Fig. 9 is pursued, where the noise is determined by P-channel MOSFETs [38].

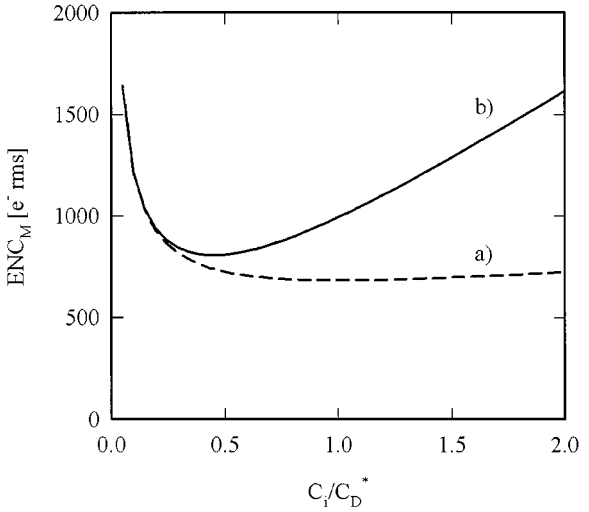

Fig. 8. ENC_M^2 as a function of the ratio C_i/C_D^* in the case of T_1 and T_2 featuring only channel thermal noise. a) Absence of T_2 noise. b) Presence of T_2 noise.

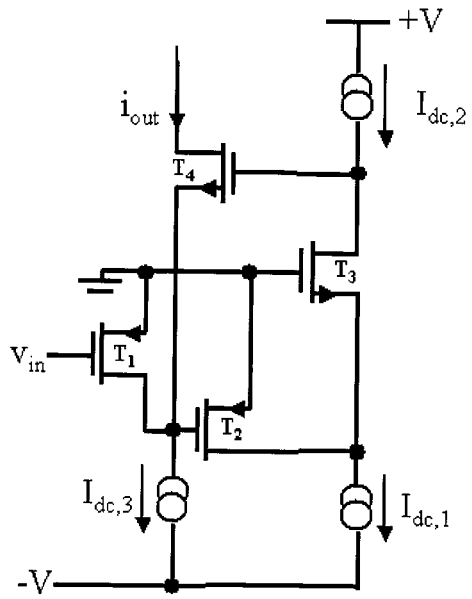

Fig. 9. Active cascode.

IV. Spectrometry Grade N-JFET Preamplifier

The upgrade in noise behavior that characterizes the CMOS processes of advanced conception has not been accompanied by a comparable progress in JFET processes. The main reason is that the monolithic JFET process used to produce the spectrometry grade N-channel devices of Figs. 3 and 4 does not allow a significant shrinking in channel length. This step would be the essential in order to increase the transition frequency of the devices and therefore improve the ENC behavior at peaking times below 100 ns.

It is necessary, however, to point out some peculiar advantages of JFETs besides their unsurpassed noise behavior in the low-frequency region. One of them is the possibility of actuating a nonresistive charge reset in a JFET by using the forward-biased gate-to-source junction or the drain feedback principle [39], [40].

V. Conclusion

The most important aspect in the optimization of the front-end design in imaging and spectrometry applications with room temperature semiconductor detectors is connected with the improvement in the noise characteristics of MOSFETs. Such an improvement is largely determined by the reduction in the thickness of the gate oxide in submicron CMOS processes. A P-channel MOSFET belonging to a technology with a submicron gate length gate and an oxide thickness in the 5-nm region behaves noisewise better than than a JFET up to peaking times of several microseconds. To take full advantage of this upgrade in the noise characteristics of active devices a careful control of the noise due to the current amplifier that follows the input device in the charge-sensitive loop becomes essential.

Acknowledgment

The authors would like to thank G. Anelli for all his help in the analysis of the noise features of submicron MOSFETs. The results on noise measurements provided by V. Speziali's group at Pavia University, Italy, is also acknowledged. The authors also thank N. Madden for his useful suggestions.

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